

**REMARKS**

**I. Introduction**

In response to the pending Office Action, Applicants have added claim 14 in order to further clarify the subject matter of the present invention. Support for claim 14 can be found, for example, in Fig. 1F through 1H and page 12, line 1 through page 13, line 5 of the specification.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art.

**II. The Rejection Of Claims 1-5 And 13 Under 35 U.S.C. § 102**

Claims 1-5 and 13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lee (U.S. No. 2003/0189215). Applicants respectfully submit that Lee fails to anticipate the pending claims for at least the following reasons.

With regard to the present invention, claim 1 recites, a method for fabricating semiconductor devices, the method comprising the steps of: forming a semiconductor layer containing a positive layer on a mother substrate; forming a metal layer on the semiconductor layer; separating the mother substrate from the semiconductor layer after forming the metal layer; and removing a desired region of the metal layer from an exposed surface of the semiconductor layer from which the mother substrate has been separated to form a plurality of mutually separated semiconductor devices each containing the semiconductor layer.

Lee discloses in paragraph [0049] that “dicing is beneficially accomplished using photolithographic techniques to etch through the metal support layer 156 to the bottom of the

passivation layer 162 (at the bottom of the trenches 130) and by removal of the passivation layer 162” (see, Fig. 15). In contrast to the present invention, Lee performs device isolation by etching from the metal support layer 156 side opposite to the n-GaN buffer layer 124 surface side that is exposed after the sapphire substrate 122 has separated from the buffer layer 124. Thus, the side exposed in Lee does not correspond to the side exposed in the present invention, which etches on the GaN buffer layer 2 side (see, Fig. 1E-1H of the present invention). As a result of this difference, it is impossible to see the layer serving as an underlying layer of the metal support layer 156 at the time of patterning and as a result, the mask alignment is difficult and the yield decreases. Thus, Lee fails to disclose a method for fabricating semiconductor devices by removing a desired region of the metal layer from an exposed surface of the semiconductor layer from which the mother substrate has been separated.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and at a minimum, Lee does not disclose a method for fabricating semiconductor devices by removing a desired region of the metal layer from an exposed surface of the semiconductor layer from which the mother substrate has been separated, it is clear that Lee does not anticipate claim 1 of the present invention.

### **III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable**

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*,

**Application No.: 10/849,823**

819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

#### **IV. Conclusion**

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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